WEST Search History

DATE: Monday, March 24, 2003

Set Name side by side	Query	Hit Count	Set Name result set
	DB=USPT,PGPB,JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=ADJ		
L22	('6032274')[ABPN1,NRPN,PN,TBAN,WKU]	2	L22
L21	l20 and clock edge with (compress$3 or compact$3) same (ic or (integrat$3 near2 circuit$3) or semi$1conduct$7 or memor$7 or stor$4 or register$4)	6	L21
L20	l19 and clock edge with (compress$3 or compact$3)	11	L20
L19	clock edge	4895	L19
L18	(L15 and L16) AnD ((@pd > 20020930)!)	0	L18
L17	(L15 and (compress$4 or compact$4) same (pull$1up or pull$1down)same latch$4 same (ic or (integrat$3 near2 circuit$3) or semi$1conduct$7 or memor$7) and (clock or timing)same (test$3 or debug$4 or verif$7 or diagno$5 or probing or probe or exerci$4)) AnD ((@pd > 20020930)!)	0	L17
L16	(L14 and (compress$4 or compact$4) same (pull$1up or pull$1down)same latch$4 same (ic or (integrat$3 near2 circuit$3) or semi$1conduct$7 or memor$7) and (clock or timing)same (test$3 or debug$4 or verif$7 or diagno$5 or probing or probe or exerci$4)) AnD ((@pd > 20020930)!)	0	L16
L15	(L14 and (compress$4 or compact$4) and (pull$1up or pull$1down)same latch$4 same (ic or (integrat$3 near2 circuit$3) or semi$1conduct$7 or memor$7) and (clock or timing)same (test$3 or debug$4 or verif$7 or diagno$5 or probing or probe or exerci$4)) AnD ((@pd > 20020930)!)	0	L15
L14	(L13 and (compress$4 or compact$4) and (pull$1up or pull$1down)same latch$4 same (ic or (integrat$3 near2 circuit$3) or semi$1conduct$7 or memor$7) and (clock or timing)) AnD ((@pd > 20020930)!)	2	L14
L13	((compress$4 or compact$4) and (pull$1up or pull$1down)same latch$4) AnD ((@pd > 20020930)!)	37	L13
L12	(L1 and (pull$1up or pull$1down)same latch$4) AnD ((@pd > 20020930)!)	0	L12
L11	(L7 and (pull$1up or pull$1down)same latch$4) AnD ((@pd > 20020930)!)	0	L11
L10	((pull$1up or pull$1down)same latch$4) AnD ((@pd > 20020930)!)	171	L10
L9	(('6163491')[ABPN1,NRPN,PN,TBAN,WKU]) AnD ((@pd > 20020930)!)	0	L9
	(L7 and double data rate same (compress$4 or compact$4) same (test$3		

L8	or debug$4 or verif$7 or diagno$5 or probing or probe or exerci$4) same (ic or (integrat$3 near2 circuit$3) or semi$1conduct$7 or memor$7) and (clock or timing)) AnD ((@pd > 20020930)!)	1	L8
L7	(L6 and double data rate and (compress$4 or compact$4) same (test$3 or debug$4 or verif$7 or diagno$5 or probing or probe or exerci$4) same (ic or (integrat$3 near2 circuit$3) or semi$1conduct$7 or memor$7) and (clock or timing)) AnD ((@pd > 20020930)!)	5	L7
L6	(double data rate and (compress$4 or compact$4) same (test$3 or debug$4 or verif$7 or diagno$5 or probing or probe or exerci$4) same (ic or (integrat$3 near2 circuit$3) or semi$1conduct$7 or memor$7)) AnD ((@pd > 20020930)!)	6	L6
L5	(L1 and (double near (data or rate) or ddr)same (compress$4 or compact$4) same (test$3 or debug$4 or verif$7 or diagno$5 or probing or probe or exerci$4) and (ic or (integrat$3 near2 circuit$3) or semi$1conduct$7 or memor$7)) AnD ((@pd > 20020930)!)	1	L5
L4	(('6324602')[ABPN1,NRPN,PN,TBAN,WKU]) AnD ((@pd > 20020930)!)	0	L4
L3	(('6317372')[ABPN1,NRPN,PN,TBAN,WKU]) AnD ((@pd > 20020930)!)	0	L3
L2	(L1 and (double near (data or rate) or ddr)same (compress$4 or compact$4) same (test$3 or debug$4 or verif$7 or diagno$5 or probing or probe or exerci$4) same (ic or (integrat$3 near2 circuit$3) or semi$1conduct$7 or memor$7)) AnD ((@pd > 20020930)!)	1	L2
L1	((double near (data or rate) or ddr)same (compress$4 or compact$4)) AnD ((@pd > 20020930)!)	13	L1

END OF SEARCH HISTORY

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L21: Entry 4 of 6 File: USPT Feb 29, 2000

DOCUMENT-IDENTIFIER: US 6032274 A
TITLE: Method and apparatus for compressed data testing of more than one memory array

Brief Summary Text (12):
One of the memory devices 16a is shown in block diagram form in FIG. 2. The memory device 16a includes a clock divider and delay circuit 40 that receives a master clock signal CKEXT and generates an internal clock signal CKINT and a large number of other clock and timing signals to control the timing of various operations in the memory device 16. The memory device 16 also includes a command buffer 46 and an address capture circuit 48 which receive an internal clock signal CKINT, a command packet CA0-CA9 on a 10-bit command bus 50, and a FLAG signal on line 52. As explained above, the command packet contains control and address information for each memory transfer, and the FLAG signal identifies the start of a command packet which may include more than one 10-bit packet word. In fact, a command packet is generally in the form of a sequence of 10-bit packet words on the 10-bit command bus 50. Each of the 10-bit packet words is received on a respective clock edge (rising or falling) of the master clock CKEXT. Thus, a 40-bit packet is typically received at four clock edges, i.e., over two cycles of the master clock CKEXT.

Brief Summary Text (27):
Each of the memory devices has a programmable latency, that defines the timing of the respective internal data clock. Upon initialization of testing, the latency of each memory device in a group is established with a distinct latency. A test read command is provided to the memory device at a first time and occupies a plurality of clock edges. Responsive to the test read command, each of the output drivers supplies either data or an error indicator at a unique edge of the respective internal data clock. The test outputs from a plurality of memory devices are provided to the test system at sequential edges of the clock in response to a single command. Compressed test data can thus be read at successive clock edges despite the command requiring a plurality of clock edges.

Detailed Description Text (17):
Where the command packet COM includes four command words, the memory controller 544 groups the devices 170a-170d, 170e-170h are grouped into groups of four. Then, each device 170 in the group receives a respective command that establishes the latencies of the devices 170 so that the devices 170 output their data at successive clock edges responsive to a single command packet COM. For example, if the uppermost device 170a in the first group outputs data at an Nth clock edge following a command, the next device 170b will output data at the (N+1)th clock edge following a command.

Detailed Description Text (18):
Once the testing timing is established, each device 170a-170d, 170e-170h in a group receives a read command including a read address with default identification data that are accepted as valid by all four devices 170a-170d or 170e-170h in the group. In response to the single read command, all four devices transfer data to their respective output registers 179. At the established clock edges, the output buffers 183 output either the valid data from the first register 179 or the tri-state condition. Thus, the four devices 170a-170d in the first group output valid data or error data at clock edges N, N+1, N+2, N+3 following the read command. Since each device 170a-170d has a different latency, each device 170a-170d outputs data at a separate clock edge and the data do not collide on the data bus 130. Also, because each bit of data indicates the status of 4 memory locations, data for 16 memory locations are output on only 4 clock edges responsive to a single command packet

COM.

CLAIMS:

15. The method of claim 14 wherein the step of outputting data from a first of the devices at a first latency relative to the issued command includes the steps of:

determining, within the first memory device, if any of the read data in the plurality of read data correspond to an error;

if any of the read data in the plurality of read data correspond to an error, producing a flag signal having a first logic state indicating the presence of an error and a second logic state indicating the absence of an error;

transferring the flag signal to an output driver circuit;

if the flag signal has the second logic state, outputting the read data responsive to a clock edge defined by the first latency; and

if the flag signal has the first logic state producing an error indicator with the output driver circuit at the clock edge defined by the first latency.

16. The method of claim 15 wherein the step of outputting data from a second of the devices at a second latency relative to the issued command includes the steps of:

reading data from the memory array in the second memory device responsive to the command;

determining, within the second memory device, if any of the read data from the memory array in the second memory device correspond to an error;

if none of the read data from the memory array in the second memory device correspond to an error, outputting the read data responsive to a clock edge defined by the second latency; and

if any of the read data from the memory array in the second memory device correspond to an error, outputting the outputting an error indicator responsive to the clock edge defined by the second latency.

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L21: Entry 5 of 6 File: USPT Feb 2, 1999

DOCUMENT-IDENTIFIER: US 5867409 A
TITLE: Linear feedback shift register

Brief Summary Text (29):
The foregoing linear feedback shift register can effectively be applied to the BIST for LSI. For example, in a recent LSI, groups of flip-flops are arranged in a boundary scanning circuit and operated in synchronization with a plurality of clock signals. Since these flip-flops are so operated, signature compression can be achieved at different clock edges as well as system clock edges of the LSI. Consequently, a delay in AC output of a DUT can be detected when the register is applied to an I/O terminal section of the LSI. Such a delay cannot be detected in a linear feedback shift register whose flip-flops are synchronized only with system clocks.

Detailed Description Text (44):
Strictly speaking, the circuit block of this example is considerably improved by signature compression at the three clock edges, as compared with a conventional one, but it is somewhat difficult to correctly check a delay in AC output of the DUT. To attain a more precise time resolution, a clock signal CLK having a higher frequency than in the above embodiments has to be generated by the PLL circuit in the circuit block 56, and the pulse width between the clock edges has to be decreased.